

REMARKS

Claims 1 and 4-8 remain pending in the above-referenced application and are submitted for the Examiner's reconsideration.

With respect to the rejection of claims 1-8 as failing to provide an enabling disclosure, in view of the amendment to claim 1 replacing "printed circuit board" with "conductor paths", Applicants submit that this rejection has been obviated.

Claims 1 and 3-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent No. 6,406,939 to Lin. Lin teaches a flip-chip connection in which so-called via holes 408 are drilled in substrate 405 by drilling. Substrate layer 405 is subsequently fastened to integrated circuit 401. Thereafter, a terminal pad 402, that is already seeded and coated in the region of connection, is further coated in such a way that via holes 408 situated to lie above it are filled up (Figure 4d). This filling up is raised up in a manner such that the upper layer of copper 406 is contacted. From the cited document of Lin, nothing is known of contacting exactly such a via using a gold bonding wire. Accordingly, withdrawal of this rejection is requested.

Claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin in view of United States Published Patent Application No. 2003/0080392 to Zuniga-Ortiz. Again, from Zuniga-Ortiz it is, among other things, not known that one can connect chip 201, using its outer metallic layers 207, to an additional electrical component in such a way that a gold bonding wire is fastened to the metallic layer 207. Rather, in paragraph 10 of Zuniga-Ortiz it is described that chip 201 is to be fastened to a wiring board by either direct welding by metallic interdiffusion, soldering or the use of conductive adhesives.

Accordingly, Applicants request that the present application issue as early as possible.

Respectfully submitted,

KENYON & KENYON LLP
R: LG (R. No. 44,172)

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By GC

Gerard A. Messina
(Reg. No. 35,952)

One Broadway
New York, New York 10004
(212) 425-7200